Two Pulse Height Discriminator Circuits

Described in this paper are a discriminator circuit and a single channel analyzer (SCA) circuit for use with a charge sensitive amplifier with a pulse shaper output. The circuits were designed to be integrated with a detector and preamplifier to make a self-contained unit requiring only an external scaler. Both circuits require positive input pulses from a charge sensitive amplifier/pulse shaper circuit.

Simple Discriminator Circuit

Figure 1 shows a discriminator circuit that generates an output pulse when the input signal level exceeds a preset threshold. The heart of this circuit is comparator U4. U4 compares a positive input pulse with a positive DC reference level. The comparator output transitions from high to low when the input level exceeds the reference level. The DC reference level is provided by shunt regulator U2. U2 is driven by an adjustable voltage regulator (U1) configured as a 10 ma current source. U1 buffers U2 from any changes in the positive supply voltage. A simpler implementation of this circuit would use a resistor instead of U1 and R1. Resistors R2, R3, and R4 set the voltage across U2 to precisely 5V. R3 is used for initial setting of the voltage reference, and is not touched during normal operation. A setup requiring more dynamic range could be accomplished by changing R2 from 4.99K to 6.04k, and R4 from 4.99k to 2k. These changes change the reference voltage to 10V rather than 5V. R5 is a 10-turn potentiometer used to adjust the voltage reference level applied to the non-inverting input of comparator U4. C2 filters wiper noise. U3A is a unity gain voltage buffer implemented with a low offset jfet - input operational amplifier. This voltage follower buffers the voltage set at R5. U3 is a non-inverting input buffer. Gain is set to 5 via R8 and R7. If necessary, varying R8 can set other gain values, or the amplifier can be converted to a unity gain buffer by omitting R7. Use of this particular amplifier for input buffer assumes input from a charge sensitive amplifier and pulse shaper. Faster input signals are not suitable for this discriminator circuit, as a relatively low speed, high precision comparator is used.
R10 and R11 apply a small amount of positive feedback around comparator U4, so that the rising and falling trip points are different. This effect is commonly known as hysteresis, and it prevents the comparator from oscillating at transitions when a relatively slow signal is applied to the inverting input. U5 generates a 5V supply from the 15V rail. R12 pulls the U4 output up to the 5V supply. U6 is a monostable circuit that puts out a 200nsec pulse when driven by the falling edge of U4. R13 and C7 determine pulse length. After delivering a pulse, the monostable remains inactive as long as the U4 output remains low. When U4 transitions back to the high state, R13 discharges C7, and the monostable can accept another input pulse. The monostable output at U6B triggers U7, which delivers a 2usec-output pulse. Q1 and Q2 buffer the U7 output so that long cables can be driven without loading down U7. Experimenters desiring a lower parts count can omit U7, and drive Q1 and Q2 from the output of spare gate U6C. If this is done, C7 should be increased to 470pF, so that the resulting output pulse is approximately 2 microseconds. Figure 2 shows the input and output waveforms from the discriminator circuit. For testing, the discriminator was driven with a pulse generator, followed by a cascaded RC differentiator and integrator. This combination provides a pulse similar to the output of a charge sensitive amplifier and pulse shaper, reducing bench clutter during testing. Since the discriminator output is loaded only with the impedance of an oscilloscope probe, the output does not return immediately to zero volts after an output pulse.

Single Channel Analyzer (SCA)

Figure 3 shows a single channel analyzer (SCA). This circuit delivers an output pulse when the input voltage falls between preset upper and lower threshold voltage levels. As in the simple discriminator circuit, the DC reference level is provided by a variable shunt regulator (U2) driven by a current source (U1, R1). R2, R3, and R4 set the maximum DC reference level to 10V. R3 is used for initial fine adjustment. Ten-turn wirewound potentiometers R5 and R8 set the upper and lower threshold levels, respectively. C3 and C5 filter potentiometer wiper noise. U3A and U3B are unity gain followers that buffer the output of each threshold adjust potentiometer. Operational amplifier U4 is set to a non-inverting

gain of five by R12 and R13, and serves to boost the input pulse. This gain can be easily changed to accommodate a different detector setup. U5 and U6 are the upper and lower threshold comparators, respectively. R6, R15, R9, and R17 provide hysteresis around each comparator to prevent oscillation during output transitions. U7 generates a +5V supply from the +15V rail to power U8 and U9. R16 and R18 pull the outputs of U5 and U7 up to +5V.
This circuit is designed so that an output pulse is generated when the input level is between the upper and lower threshold levels. The pulse occurs when input pulse voltage passes back though the preset lower threshold voltage. When no input is present, the output of each threshold comparator is high, and the output of U8D is low. U6A and U6B form a cross-coupled latch. The low output from U8D, along with the high output from U5, sets this latch such that the output at U8B is high. If a pulse appears that is between the upper and lower threshold levels, the U6 output is low, and U5 output is high (5V). The U8D output is high and the cross couple latch formed by U6A and U6B does not change state. When the pulse passes back through the lower threshold voltage, U6 transitions from the low state back to a high state. A 700 nsec positive pulse is generated by differentiator C17 and R22, and is applied to NAND gate U8C. Since the other side of the gate is high, a low pulse is generated at the output of U8C, triggering U9.

If the pulse exceeds both lower and upper thresholds, U5 transitions to the low state and the latch changes state, changing the output of U8B to the low state. This locks the U8C output in the high state, so that it cannot respond to any trigger pulses generated when U6 transitions back to the high state. This prevents U9 from triggering. R20 and C14 store the U8B low state so that its persists until the pulse from C17 and R22 decays.
U9 is configured as a monostable multivibrator. R24 and C16 set the output pulse width to 1usec. Q1 and Q2 buffer the U9 output.
Circuit performance is shown in Figures 4-6. The input was driven with a pulse generator followed by a cascaded RC differentiator and integrator to simulate the output of a charge sensitive amplifier with pulse shaping. Figure 4 shows the input waveform and the output of preamplifier U4. Figure 5 shows output of preamplifier u4, the output the upper and lower threshold comparators, and the main output. The threshold levels are set such that the input pulse falls between the upper and lower thresholds. As can be seen, only the lower threshold comparator is active, and an output pulse is generated at the rising edge of the lower threshold comparator output. Figure 6 shows the same setup, except the upper threshold level has been adjusted downward so that the upper threshold comparator is also triggered. As can be seen, the output pulse is inhibited.

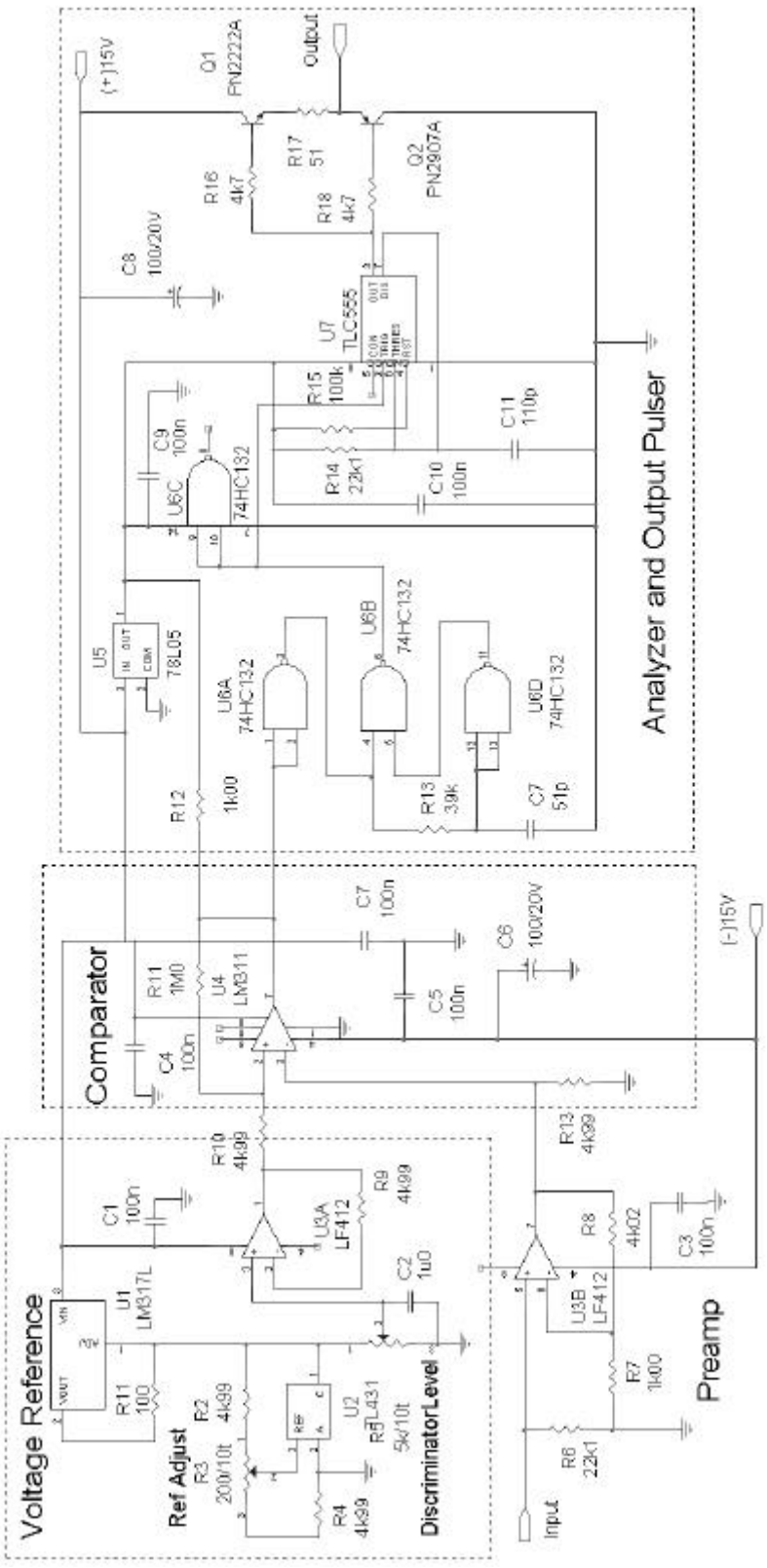

Figure 1. Simple Discriminator Circuit

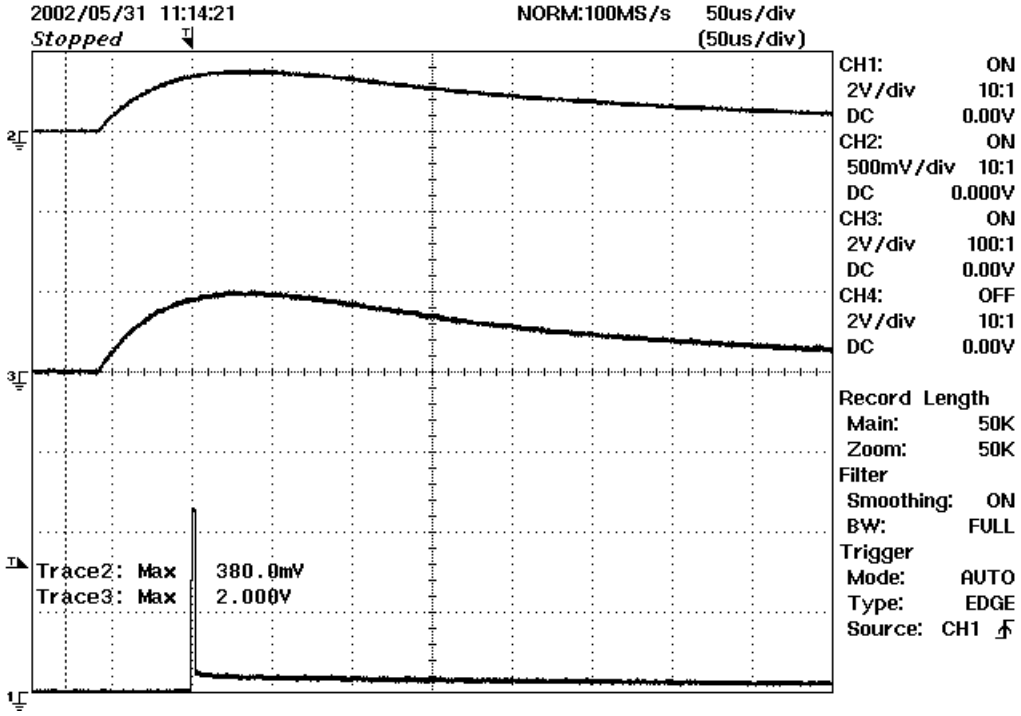

Figure 2. Input and Output Waveforms for simple Discriminator Circuit
Middle Trace: Input Pulse, 200 mV/ div, 50 usec/div
Top Trace: Discriminator Preamp Output, 2V/ div, 50 usec/div
Bottom Trace, Discriminator Output Pulse, 2V/div, 50usec/div

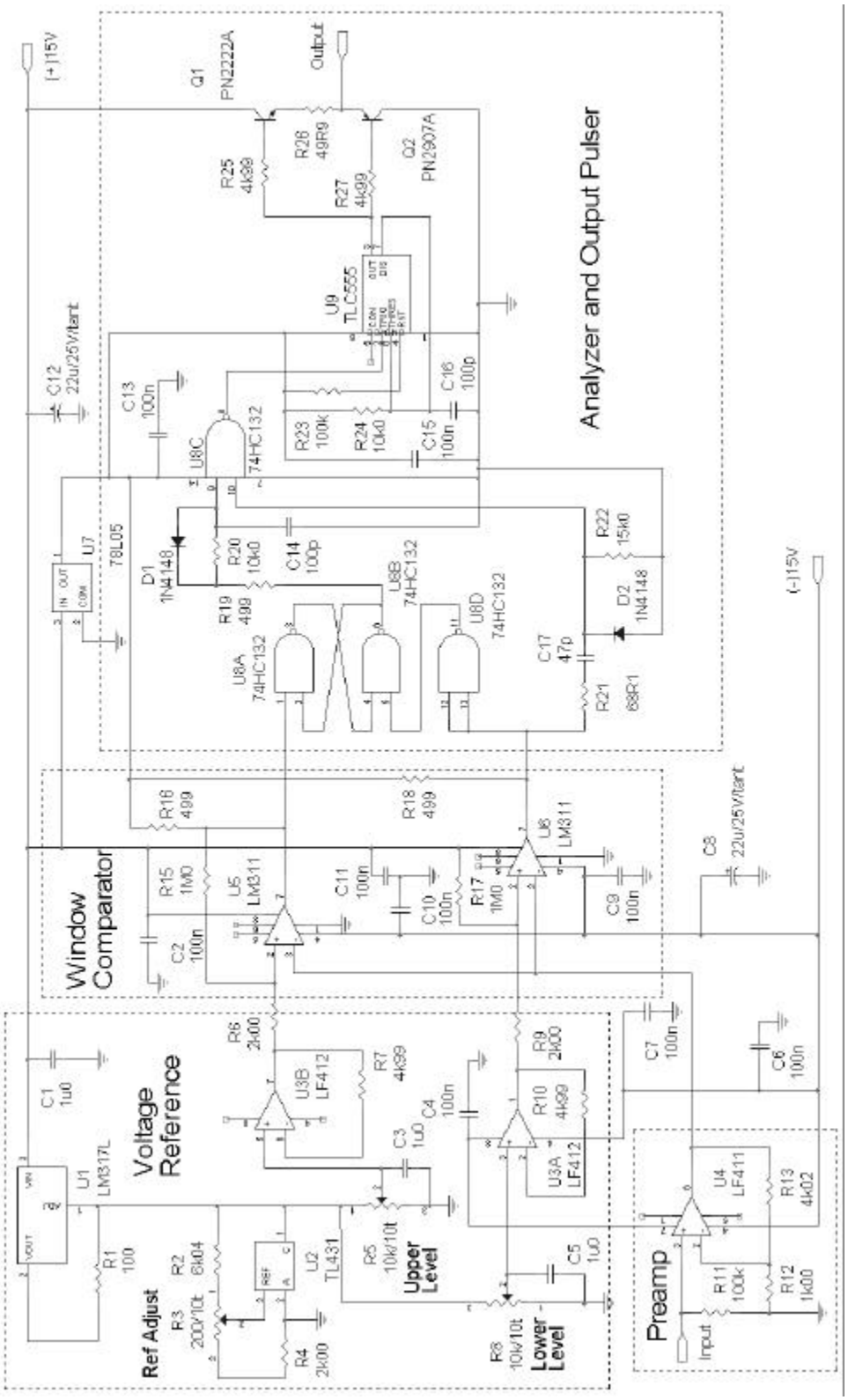

Figure 3. Single Channel Analyzer (SCA) Circuit

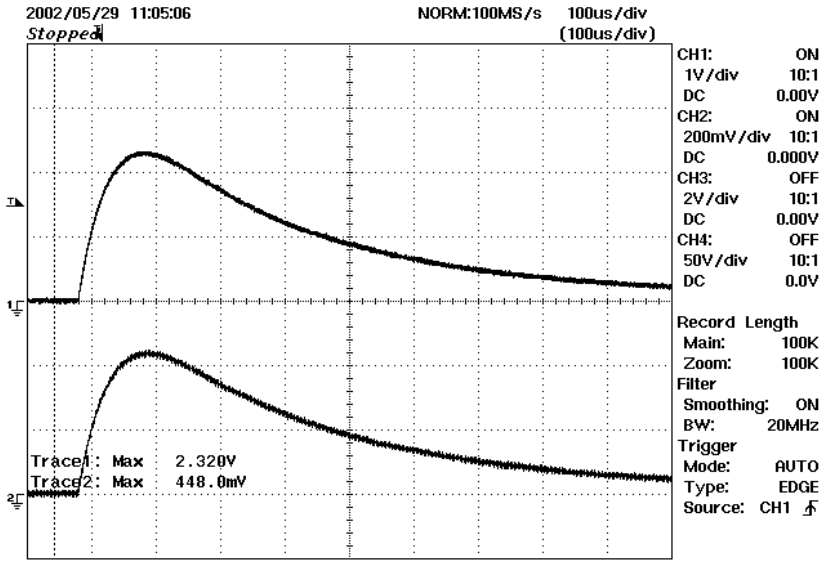

Figure 4. Input Waveform and SCA Preamp Output
Trace 2: SCA Input, 200mV/div, 100usec/div
Trace 1: SCA Preamp Output, 1V/div, 100usec/div

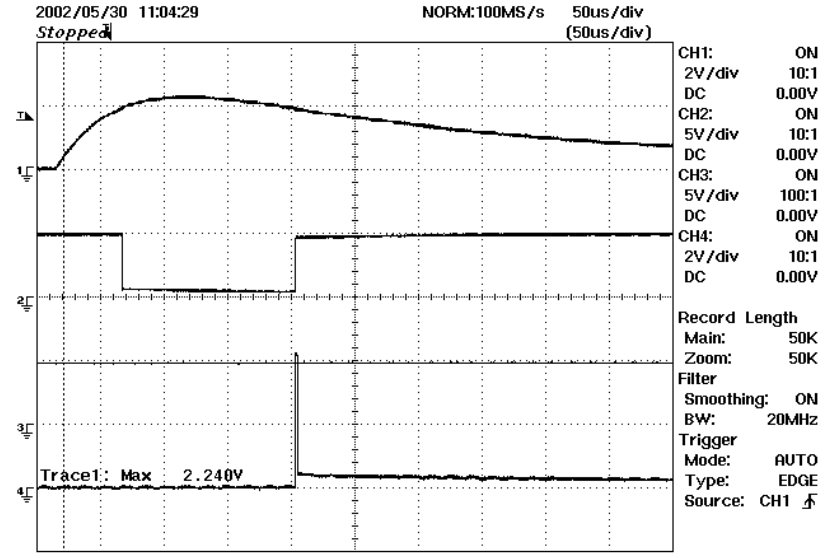

Figure5. SCA Output with Lower Threshold Triggered
Trace 1: SCA Preamp Output, 2V/div, 50 usec/div
Trace 2: Lower Threshold Comparator Output, 5V/div, 500usec/div
Trace 3: Upper Threshold Comparator, 5V/div, 50usec/div
Trace 4: SCA Output, 2V/div, 50 usec/div

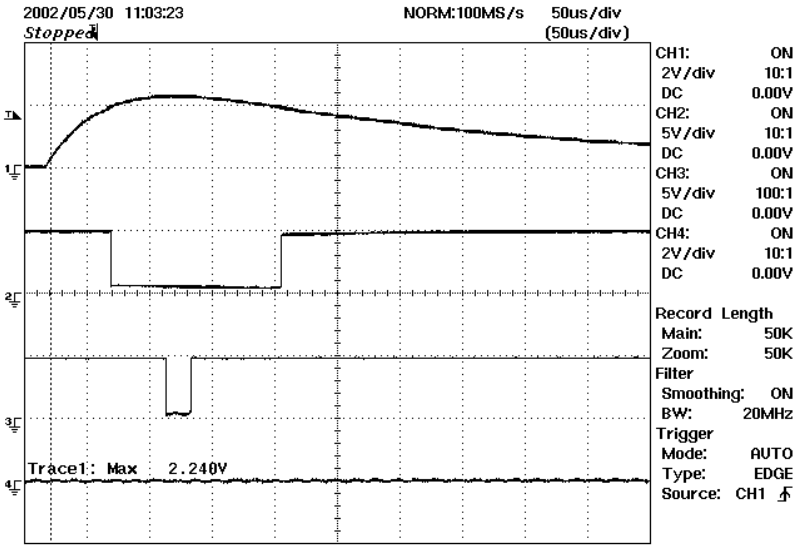

Figure 6. SCA Output with both Lower and Upper Threshold Triggered
Trace 1: Preamp Output, 2V/div, 50 usec/div
Trace 2: Lower Threshold Comparator Output, 5V/div, 500usec/div
Trace 3: Upper Threshold Comparator, 5V/div, 50usec/div
Trace 4: SCA Output, 2V/div, 50 usec/div